AMENDMENTS TO THE CLAIMS

1. (Currently amended) A DMA controller comprising:

a plurality of DMA channels, each including a datapath for transferring data from a DMA source to DMA destination and channel control logic for controlling data transfer in response to DMA parameters; and

a prioritizer configured to map DMA requests from different DMA requesters to the DMA channels in response to programmable mapping information, wherein the prioritzer comprises a priority crossbar configured to map inputs to outputs based on the programmable mapping information, wherein the priority crossbar is configured to map DMA requests and DMA grants in response to programmable mapping information associated with each of the DMA channels.

2. (Canceled)

3. (Currently amended) A DMA controller as defined in claim [[2]]1, wherein the priority crossbar includes conflict resolution circuitry configured to ensure that each input is mapped to only one output.

4-6. (Canceled)

7. (Currently amended) A method for DMA transfer, comprising:

providing a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination;

controlling data transfer through each of the channels in response to DMA parameters; ~~and~~

mapping DMA requests from different DMA requesters to the DMA channels in response to programmable mapping information; and

mapping DMA grants from the DMA channels to respective DMA requesters, wherein mapping DMA requests and mapping DMA grants comprises mapping DMA requests and grants with a priority crossbar.

8. (Canceled)

9. (Canceled)

10. (Original) A method as defined in claim 7, further comprising resolving conflicts so that each of the DMA requests is mapped to only one of the DMA channels.

11. (Original) A method as defined in claim 8, wherein mapping DMA requests and mapping DMA grants is responsive to programmable mapping information associated with each channel.

12. (Currently amended) A DMA controller comprising:

a plurality of DMA channels, each including a datapath for transferring data from a DMA source to a DMA destination and channel logic for controlling data transfer in response to DMA parameters;

a first prioritizer configured to arbitrate among DMA requests in accordance with a predetermined assignment of priorities; and

a second prioritizer configured to map DMA requests from different DMA requesters to the DMA channels in response to programmable mapping information, wherein the second prioritizer comprises a priority crossbar configured to map DMA requests to the DMA channels and configured to map DMA grants to respective DMA requesters.

13. (Canceled)

14. (Currently amended) A DMA controller in defined in claim [[13]]12, wherein the priority crossbar includes conflict resolution circuitry configured to ensure that each input is mapped to only one output.

15. (Original) A DMA controller as defined in claim 12, wherein the second prioritizer is configured to map DMA grants to respective DMA requesters in response to the programmable mapping information.